IN THE CLAIMS

1-17 (Canceled).

18. (New) A data processor formed on a semiconductor substrate which is connectable to a synchronous memory, comprising:

a data processing unit;

a display unit;

an image input unit;

each of the units having a priority order which indicates a memory access priority order,

a plurality of registers, and at least one of which stores an initial set value according to the priority order;

a control unit controlling arbitration to access to the synchronous memory, and allowing to one of the data processing unit, display unit and image input unit access to the synchronous memory; and

a plurality of timer units which are set at a initial set value according to the priority order,

wherein each of the data processing unit, display unit, and image input unit provides an access request to the control unit to access the synchronous memory,

wherein the control unit allows one of the units which provide access requests to access the synchronous memory according to the value of the timer unit.

19. (New) The data processor according to claim 18,

wherein the timer units perform a count-down operation,

wherein one timer unit starts the count-down operation, when the control unit receives the access request corresponding to the units accessing the synchronous memory,

wherein the initial set value of a module having high priority order is smaller than the initial set value of a module having low priority order, and

wherein the control unit allows, to the unit outputting the access request, access to the synchronous memory, when the timer unit of the unit outputting the access request has the low value.

20. (New) The data processor according to claim 19,

wherein the display unit has a high priority order, and the image input unit has a low priority order, and

wherein the initial set value of the high priority order is smaller than that of the low priority order.

21. (New) The data processor according to claim 18,

wherein the data processing unit further comprises a memory interface unit operating to access the synchronous memory, and outputting the data signals, address signals and

control signals, and inputting data signals to the synchronous memory, and

wherein the memory interface unit controls access to the synchronous memory according to arbitration of the control unit.